

Architecture

STM32H723ZG main MCU software architecture - layers, state machine, FOC, modulation, sensing, and safety mechanisms.

Document ID	OV-SW-MAINMCU-ARCH
Version	0.1
Date	2026-08-08
Status	draft
Applies to	openvvvf-control-module, software-target-main-mcu
Product line	openvvvf
Normative references	OV-SAF-HARA-CORE, OV-CA-SWM-INDEX

Placeholder / Under Revision - This page is incomplete or out of date and will be revised.

1. Architecture

PLACEHOLDER

- This document will define the main MCU software architecture from scratch. The old SWAD is being abandoned.

1.1. Planned sections

1. Design principles and layer model
2. System state machine
3. FOC and modulation library
4. Multi-rate ADC and current sensing
5. CAN communication and protocol model
6. Safe-state and fault management
7. Input validation and parameter storage
8. Power-loss estimator and thermal model
9. Memory layout and startup
10. Traceability to HARA FSRs