OPENVVVF

DESIGN DOCUMENT

System Thermal Analysis

IGBT and diode loss analysis, inverter efficiency, and heatsink/baseplate sizing for the Chassis Size 2 traction inverter.

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1. System Thermal Analysis

This document estimates the total heat dissipated into the heatsink by the 3-phase traction inverter power stage (3× Mitsubishi CM600DY-24T half-bridge IGBT modules plus the DC-link capacitor bank) and derives the heatsink thermal resistance required for continuous operation. It is the sizing input for the custom heatsink design.

Value marking convention used throughout:

- **[DS]** - value taken directly from the CM600DY-24T datasheet (Mitsubishi Electric, publication date December 2020); page/figure cited.
- **[EST]** - engineering estimate derived from datasheet curves (digitized) or standard scaling laws; not explicitly guaranteed by the datasheet.
- **[ASM]** - modeling assumption about the operating point.

1.1. Nomenclature

Symbol	Meaning	Units
	Cross-sectional area (generic)	m²
	Load power factor	-
	High-side switch duty cycle as a function of electrical angle	-
	IGBT turn-on switching energy per pulse	J
	IGBT turn-off switching energy per pulse	J
	Free-wheeling diode reverse-recovery energy per pulse	J
	PWM switching frequency	Hz
	Instantaneous phase current as a function of electrical angle	A
	Peak sinusoidal phase current ( )	A
	IGBT collector DC current	A
	IGBT repetitive peak collector current	A
	Free-wheeling diode forward current	A
	RMS phase current	A
	Thermal conductivity	W/(m·K)
	Length (thermal conduction path)	m
	Modulation index ( )	-
	DC-link capacitor bank heat load	W
	Free-wheeling diode conduction loss (per diode)	W
	Total heat rejected to the heatsink	W
	Heat dissipated per IGBT module	W
	Inverter output power	W

Symbol	Meaning	Units
	IGBT conduction loss (per IGBT)	W
	Total semiconductor (IGBT + FWD) loss	W
	Free-wheeling diode switching loss (per diode)	W
	IGBT switching loss (per IGBT)	W
	Heat flow / power	W
	IGBT gate charge	C
	Free-wheeling diode reverse-recovery charge	C
	IGBT on-state resistance (chip + lead)	Ω
	Free-wheeling diode on-state resistance (chip + lead)	Ω
	External gate resistance	Ω
	Module internal lead resistance	Ω
	Thermal resistance	K/W
	Module case-to-sink (baseplate-to-heatsink) thermal resistance	K/W
	Free-wheeling diode junction-to-case thermal resistance	K/W
	IGBT junction-to-case thermal resistance	K/W
	Heatsink surface-to-ambient thermal resistance	K/W
	PWM dead time	s
	Free-wheeling diode reverse-recovery time	s
	Module baseplate (case) temperature	°C
	Semiconductor junction temperature	°C
	Free-wheeling diode junction temperature	°C
	IGBT junction temperature	°C

Symbol	Meaning	Units
/	Maximum / continuous operating junction temperature	°C
	Heatsink surface temperature under the module	°C
	Ambient temperature	°C
	Module case temperature (datasheet reference)	°C
	Virtual junction temperature	°C
	DC-link voltage during switching-test conditions	V
	IGBT collector-emitter saturation voltage	V
	IGBT collector-emitter breakdown voltage	V
	DC-link voltage	V
	Free-wheeling diode forward voltage	V
	Free-wheeling diode threshold voltage (model fit)	V
	IGBT threshold voltage (model fit)	V
	Gate-emitter drive voltage	V
	Peak phase voltage	V
	RMS phase voltage	V
	Temperature rise / difference	K or °C
	Inverter efficiency	-
	Thermal conductivity (e.g., grease)	W/(m·K)
	Current phase lag behind voltage (power-factor angle)	rad
	Electrical angle	rad

1.2. References and system inputs

- CM600DY-24T datasheet, Mitsubishi Electric, December 2020 (600 A / 1200 V dual (half-bridge) IGBT module, 62 mm package).
- `OV-C2-DD-DCLINK-THERMAL` - DC-link capacitor bank heat load of ≈40 W at rated ripple, rejected to the heatsink through the standoff/spreader-plate path.
- Project README - power stage: 3× CM600DY-24T half-bridge modules (one per phase), SVPWM, default switching frequency 2 kHz (300 Hz – 16 kHz range), DC link 102–320 V (140 V nominal), 600 A class output. Gate drive +15 V / −9 V via onsemi NCV57100.

1.3. Datasheet parameters used (CM600DY-24T)

1.3.1. Ratings and electrical characteristics

Parameter	Value	Conditions	Source	Mark
	1200 V	G–E shorted	Datasheet p.2, Maximum Ratings	[DS]
(DC)	600 A		Datasheet p.2	[DS]
	1200 A	repetitive pulse	Datasheet p.2	[DS]
, chip	1.55 V typ / 1.80 V max	A, V,	Datasheet p.2, Electrical Characteristics	[DS]
, chip	1.75 V typ	A, V,	Datasheet p.2	[DS]
, chip	1.80 V typ	A, V,	Datasheet p.2	[DS]
, terminal	1.75 / 2.00 / 2.10 V typ (2.05 V max at 25 °C)	A, 25 / 125 / 150 °C	Datasheet p.2	[DS]
, chip (FWD)	1.65 V typ (2.00 V max at 25 °C)	A, 25 / 125 / 150 °C	Datasheet p.2	[DS]
, terminal (FWD)	1.85 / 2.00 / 2.00 V typ	A, 25 / 125 / 150 °C	Datasheet p.2	[DS]
	56.6 mJ typ	V, A, V, , , inductive load	Datasheet p.2	[DS]
	64.3 mJ typ	same conditions	Datasheet p.2	[DS]

Parameter	Value	Conditions	Source	Mark
	38.2 mJ typ	same conditions, A	Datasheet p.2	[DS]
/	60 µC typ / 400 ns max	V, A,	Datasheet p.2	[DS]
	3.7 µC typ	V, A, V	Datasheet p.2	[DS]
(internal lead R)	0.3 mΩ typ	per switch,	Datasheet p.2	[DS]
Switching times	ns, ns, ns, ns	V, A,	Datasheet p.2	[DS]
/	continuous / instantaneous	-	Datasheet p.2	[DS]
Recommended operating point	V typ (850 V max), V, –	-	Datasheet p.4	[DS]

1.3.2. Thermal resistances

Parameter	Value	Per	Source	Mark
	24 K/kW max (= 0.024 K/W)	one inverter IGBT	Datasheet p.3, Thermal Resistance	[DS]
	42 K/kW max (= 0.042 K/W)	one inverter FWD	Datasheet p.3	[DS]
	13.3 K/kW typ (= 0.0133 K/W)	one module (grease W/(m·K), 50 µm)	Datasheet p.3, note 6	[DS]

Note: is a typical value; no maximum is given. Grease ageing/pump-out (datasheet note 8) can raise it over life - covered by the heatsink margin policy in §6.

1.3.3. Device model parameters digitized from datasheet curves

Conduction models use the standard straight-line fit to the datasheet output/saturation curves at (chip values), with the internal lead resistance added because it dissipates heat inside the module:

Model parameter	Value	Basis	Mark
	1.15 V	Fit to vs curve, chip, 125 °C (datasheet p.6, "Collector-Emitter Saturation Voltage Characteristics"); fit passes through (300 A, 1.45 V), (600 A, 1.75 V), (900 A, 2.05 V)	[EST]
	1.0 mΩ (+ 0.3 mΩ lead = 1.3 mΩ used)	same figure + p.2 lead resistance	[EST]
	1.15 V	Fit to FWD forward curve, chip, 125 °C (datasheet p.6, "Free Wheeling Diode Forward Characteristics"); through (300 A, 1.38 V), (600 A, 1.65 V), (1200 A, 2.10 V)	[EST]
	0.8 mΩ (+ 0.3 mΩ lead = 1.1 mΩ used)	same figure + p.2 lead resistance	[EST]

Switching energy models (datasheet p.7, "Half-Bridge Switching Characteristics - switching energy vs collector/emitter current", V, V, ; the solid curves were used, anchored exactly at the p.2 table values at 600 A; the dashed 125 °C curves lie ≈5–10 % lower, so the 150 °C curves are conservative at the 125 °C operating point):

I				Mark
300 A	≈ 30 mJ (fit 28 mJ)	≈ 37 mJ	≈ 31 mJ	[EST]
600 A	56.6 mJ	64.3 mJ	38.2 mJ	[DS] anchor
850 A	≈ 106 mJ	≈ 94 mJ	≈ 39 mJ	[EST]
1200 A	≈ 180 mJ	≈ 130 mJ	≈ 39 mJ	[EST]

Piecewise-linear interpolation of these anchor points is used in the model. Digitization uncertainty is about ±5 % (line thickness / anti-aliasing). Note is markedly superlinear above 600 A, and saturates above ≈700 A.

Scaling laws applied (not given in the datasheet):

- **Voltage scaling:** . Standard first-order scaling of switching energy with bus voltage. [EST]
- **Temperature:** 150 °C energy curves used at the 125 °C operating point (conservative). Conduction parameters at 125 °C. [EST]
- **Gate conditions:** datasheet energies are at V and ; the inverter drives +15 V / −9 V. Energies are assumed equal; actual populated gate resistance must match the class or rise (datasheet p.7, vs figure: at , roughly triples). [ASM]

1.4. Loss model and assumptions

1.4.1. Assumptions [ASM]

- 3 half-bridge modules, one per phase, symmetrical sharing.
- Modulation index , defined as (within the linear SVPWM range, which extends to in this convention).
- Sinusoidal phase current with .
- Load power factor (traction motor at rated point).
- Junction operating point (continuous rating is 150 °C; 125 °C leaves margin).
- Switching frequency kHz (default); 16 kHz evaluated as worst case.
- Dead time (0.5–4 µs configurable): the extra FWD conduction during dead time adds ≈ W per leg (~20 W total) at 600 A / 2 kHz / 2 µs - under 1 % of total heat, neglected.
- Gate-drive power (W per switch, ≈1 W total) is dissipated in the gate resistors/driver, not the module - excluded.
- as measured in the datasheet half-bridge circuit already contains the turn-on impact of the opposing diode's reverse recovery; is counted once, in the diode (standard datasheet convention).

1.4.2. Formulas

High-side fundamental duty cycle of one leg (identical for SPWM and SVPWM to first order; third-harmonic injection does not change the fundamental average that sets the IGBT/FWD conduction split):

Conduction loss per IGBT and per FWD (standard 2-level bridge result, integrating over the positive current half-wave):

Switching loss, averaging the digitized energy curves over the sine half-wave and scaling with bus voltage:

Totals for the bridge (6 IGBTs + 6 FWDs) and the heatsink:

Per-module dissipation (for the thermal chain):

1.5. Heat vs phase current

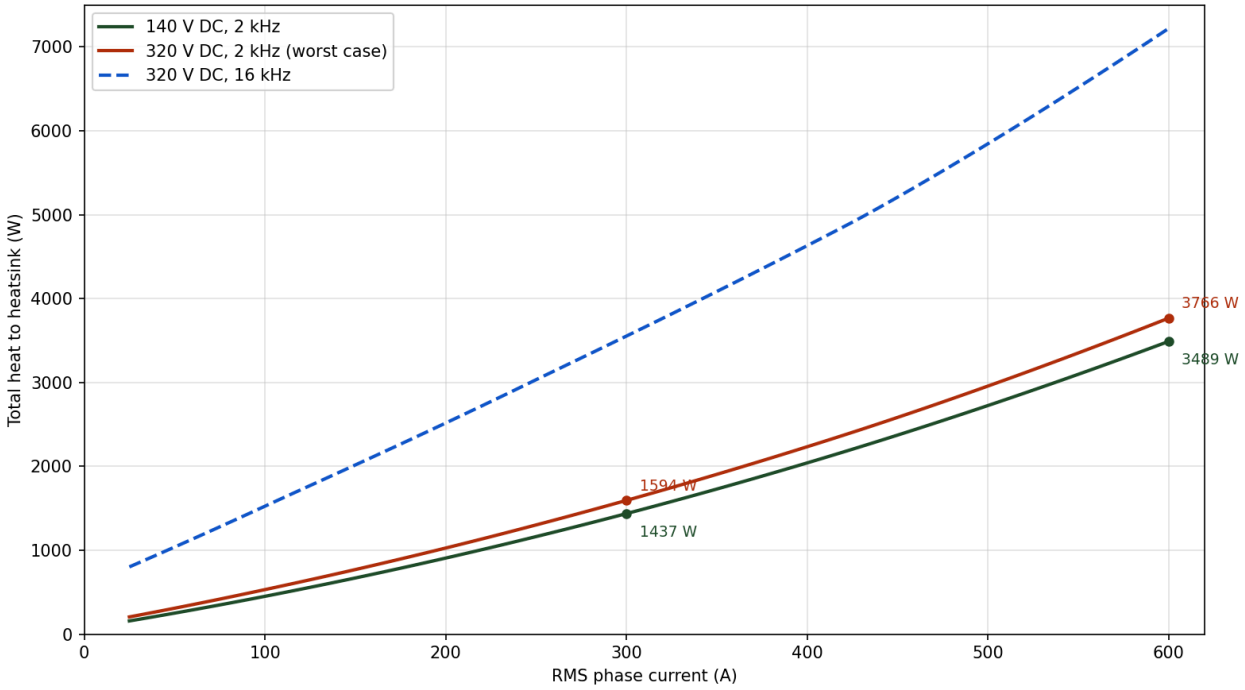
Total heat rejected to the heatsink (IGBT + FWD conduction and switching, plus 40 W capacitor heat), 2 kHz, , :

(A rms)	IGBT cond., 6× (W)	FWD cond., 6× (W)	Switching, 6× @140 V (W)	Caps (W)	Total @140 V / 2 kHz (W)	Total @320 V / 2 kHz (W)	Total @320 V / 16 kHz (W)
50	135	30	46	40	250	309	1038
100	286	63	62	40	451	531	1525
150	453	99	78	40	669	770	2016
200	637	137	93	40	906	1026	2516
250	837	177	108	40	1162	1301	3032
300	1053	221	122	40	1437	1594	3552
350	1286	267	136	40	1729	1904	4084
400	1535	316	150	40	2041	2233	4630
450	1801	367	164	40	2372	2583	5208
500	2083	421	180	40	2724	2957	5845
550	2381	478	198	40	3097	3351	6517
600	2696	537	216	40	3489	3766	7219

Conduction dominates at 2 kHz (switching is only ≈6 % of semiconductor loss at 140 V / 600 A because the energies scale with). At 320 V / 16 kHz switching becomes dominant (≈3.9 kW of the 7.2 kW at 600 A).

Loss breakdown at the two design currents (140 V, 2 kHz):

Quantity	300 A rms	600 A rms
Per-IGBT conduction	176 W	449 W
Per-FWD conduction	37 W	89 W
Per-IGBT switching	14 W	28 W
Per-FWD switching ( )	7 W	8 W
Per module ( )	466 W	1150 W
Semiconductor total	1397 W	3449 W
Total to heatsink (incl. 40 W caps)	**1437 W**	**3489 W**



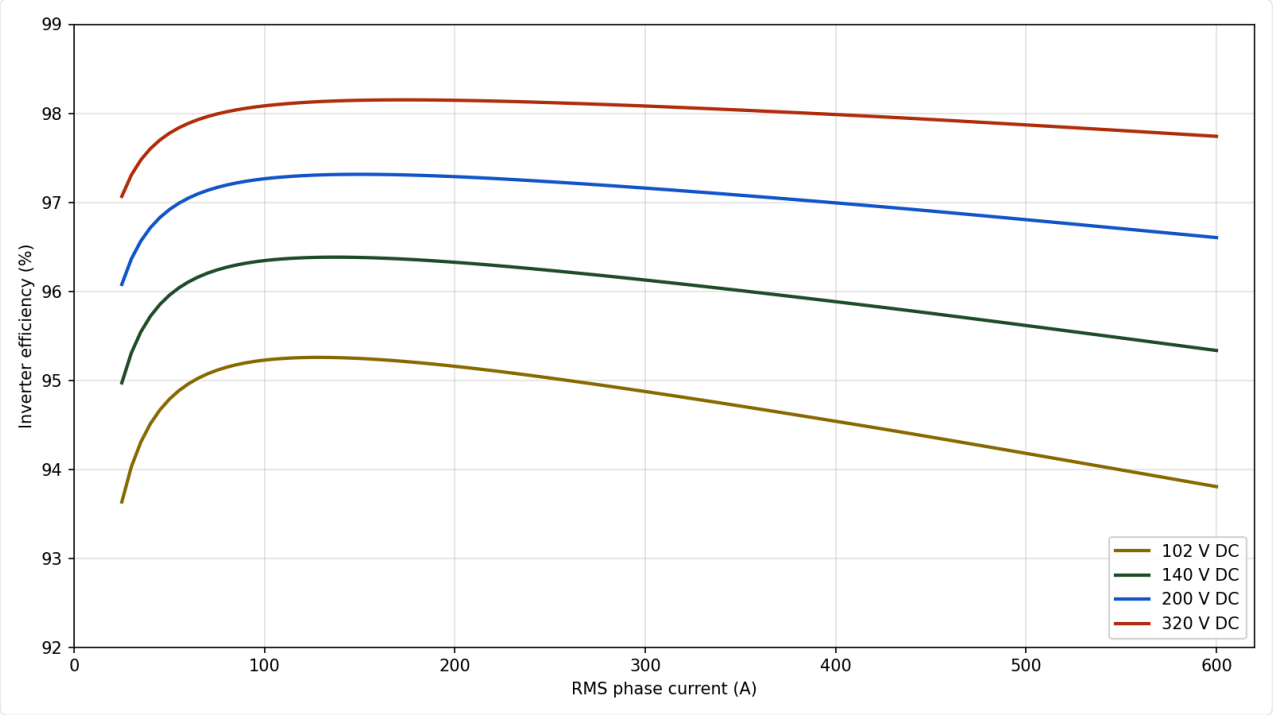
1.6. Inverter efficiency vs phase current

including the 40 W capacitor heat.

i.e., each bus voltage runs at its rated fundamental output voltage (at 600 A: 52 kW @102 V, 71 kW @140 V, 102 kW @200 V, 163 kW @320 V).

(A rms)	@102 V (%)	@140 V (%)	@200 V (%)	@320 V (%)
50	94.8	96.0	96.9	97.8
100	95.2	96.3	97.3	98.1
150	95.2	96.4	97.3	98.1
200	95.2	96.3	97.3	98.1
250	95.0	96.2	97.2	98.1
300	94.9	96.1	97.2	98.1
350	94.7	96.0	97.1	98.0
400	94.5	95.9	97.0	98.0
450	94.4	95.8	96.9	97.9
500	94.2	95.6	96.8	97.9
550	94.0	95.5	96.7	97.8
600	93.8	95.3	96.6	97.7

At the 140 V nominal bus the efficiency peaks at ≈96.4 % around 150–200 A and falls to 95.3 % at 600 A, because conduction loss grows faster than output power (the term). Higher bus voltages are more efficient at the same current because conduction loss is unchanged while output power scales with .



1.7. Heatsink sizing

1.7.1. Thermal chain

Steady-state 1-D chain from junction to ambient for the hottest IGBT of a module:

- K/kW typ per module (thermal grease) [DS p.3]
- K/kW max, K/kW max [DS p.3]
- Design limits: module baseplate at ; junction target with margin (continuous rating 150 °C [DS]). The 85 °C baseplate limit is also consistent with the SWAD NTC monitor (100 °C hard cap on the module-sited NTC) and with the DC-link spreader plate, which reaches ≈80 °C at a 40 °C heatsink base under its 40 W load (`OV-C2-DD-DCLINK-THERMAL`).

1.7.2. Required heatsink thermal resistance

Worst case is 320 V bus (highest switching loss); 140 V nominal shown for reference, 16 kHz as the upper switching bound.

Operating point	(W)	(W)	(K)	Max (°C)	Required	check	check
300 A / 320 V / 2 kHz	1594	518	6.9	78.1	**≤ 0.0239 K/W**	90 °C ✓	87 °C ✓
600 A / 320 V / 2 kHz (design point)	3766	1242	16.5	68.5	**≤ 0.0076 K/W**	97 °C ✓	90 °C ✓
600 A / 140 V / 2 kHz (reference)	3489	1150	15.3	69.7	≤ 0.0085 K/W	96 °C ✓	89 °C ✓
600 A / 320 V / 16 kHz (reference)	7219	2393	31.8	53.2	≤ 0.0018 K/W	108 °C ✓	95 °C ✓

1.7.3. Guidance

- **Continuous 600 A (design point): K/W (7.6 mK/W) for the whole three-module heatsink assembly, 40 °C ambient.** With ≥25 % engineering margin (grease ageing, digitization/typ-value uncertainty, module-to-module variation, fouling), the design target is **≈ 0.006 K/W or better**. This is outside natural-convection territory (a very large natural-convection sink is ≈0.1–0.5 K/W); it requires a large forced-air heatsink or a liquid cold plate.
- **Continuous 300 A: K/W** - achievable with a moderate forced-air extrusion.
- The junction rise is small at the design point (at , ≈28 °C margin to the 125 °C target) because is only 24 K/kW; the **baseplate ≤ 85 °C constraint, not the junction, sizes the heatsink.** Per-switch dissipation of ≈520 W at 600 A / 320 V / 2 kHz is also well inside the module's 6250 W total dissipation rating (datasheet p.2).
- 16 kHz operation at high current is impractical with air cooling (≤1.8 mK/W needed at 600 A) and marginal even with liquid cooling; treat 16 kHz as a reduced-current mode (see §7).
- Mounting: thermal grease per datasheet note 6 (W/(m·K), 50 µm), M6 mounting torque 3.5–4.5 N·m (datasheet p.3), baseplate flatness ≤ 200 µm on the centerlines. Verify the three modules are placed so each sees comparable sink temperature.

1.8. Sensitivity and notes

- **16 kHz switching:** switching loss scales linearly with (×8 vs 2 kHz). At 600 A / 320 V total heat rises from 3.8 kW to 7.2 kW and the heatsink requirement tightens from 7.6 to 1.8 mK/W. At 300 A / 320 V / 16 kHz the total is 3.55 kW and the requirement is mK/W (same

chain) - still forced-air/liquid territory. Recommend keeping 16 kHz for light-load/low-noise operation only.

- **Lower power factor:** total heat is nearly unchanged (the IGBT term falls while the FWD share rises; at , 600 A / 140 V / 2 kHz, kW vs 3.49 kW at), but output power falls proportionally with , so efficiency drops (≈92.8 % at , 600 A / 140 V) and heat per kW delivered rises. Regenerative braking ( ) shifts loss toward the FWDs - K/kW keeps the diode junction ≈5 °C cooler than the IGBT at rated point, so this is not binding.
- **Typical vs maximum device values:** conduction uses typical chip ; the max terminal values are ≈10–15 % higher, and is a typical (not max) value. The ≥25 % heatsink margin policy covers this.
- **600 A RMS operation:** at 600 A RMS the sine peak is 848 A, above the module's 600 A DC rating (at) but within the 1200 A repetitive pulse rating. Continuous 600 A RMS is the inverter's design target (README), with full-load dyno/thermal validation still pending - treat the 600 A column as the sizing bound, not a validated continuous rating.
- **Gate resistance:** all switching energies assume the datasheet condition. If the populated gate resistance is larger, increase substantially (≈3× at 10 Ω for , datasheet p.7) - re-run this analysis if the gate design deviates.
- **Low-current extrapolation:** below ≈100 A the curve extrapolation carries the constant offsets (mJ, mJ); the resulting low-current, high-frequency numbers (e.g., 50 A / 16 kHz) are the least accurate in this document, ±15 %.
- **Not modeled:** stray-inductance overshoot losses, module NTC self-heating, busbar/terminal ohmic heating into the heatsink (small vs 3.5 kW), and heatsink thermal spreading between modules (left to the heatsink detailed design). Ambient 40 °C is assumed at the heatsink inlet; inside a sealed chassis, derate accordingly.
- **Firmware tie-in:** the real-time loss estimator uses the same model structure (conduction + curves + chain); the parameters in §2.3 are the recommended calibration set for it.

This is a design estimate for heatsink sizing, to be validated by test on the assembled inverter.